Claims

[c1] A process of fabricating a circuit structure having a micromachined member, the process comprising the steps of:
forming a circuit device on a substrate by processing steps that include forming multiple dielectric layers and at least one conductive layer on the substrate, the multiple dielectric layers comprising an oxide layer on a surface of the substrate and at least two dielectric layers that are in tension, the at least one conductive layer being between the at least two dielectric layers; and then
dry etching a surface of the substrate to form a cavity therein and thereby delineate the micromachined member and a frame surrounding the micromachined member, the dry etching step terminating at the oxide layer, the micromachined member comprising the multiple dielectric layers and the at least one conductive layer.

[c2] The process according to claim 1, wherein the micromachined member is a diaphragm having a perimeter supported by the frame.

[c3] The process according to claim 2, wherein the diaphragm has a first surface for receiving thermal radiation and a sensing layer that contains at least a pair of interlaced thermopiles, each thermopile comprising a sequence of thermocouples, each thermocouple comprising dissimilar electrically-resistive materials that define hot junctions located on the diaphragm and cold junctions located on the frame, the at least one conductive layer defining metal conductors that electrically connect the thermopiles to the circuit device.

[c4] The process according to claim 3, further comprising the step of forming a metal body so as to be within the diaphragm for reflecting thermal energy through at least one of the multiple dielectric layers toward the hot junctions of the thermopiles.

[c5] The process according to claim 3, further comprising the step of forming a metal body so as to be within the diaphragm, surrounding the hot junctions of the thermopiles, and between the hot and cold junctions of the thermopiles, the metal body serving to equalize thermal energy at the cold junctions.

[c6] The process according to claim 3, wherein one of the dissimilar electrically-resistive materials is p-type doped polysilicon.

[c7] The process according to claim 1, wherein the cavity has a rectangular shape with rounded corners.

[c8] The process according to claim 1, wherein at least one dielectric layer of the multiple dielectric layers is formed of an infrared-absorbing material chosen from the group consisting of an oxynitride or a tetra-ethyl-ortho-silicate based oxide.

[c9] The process according to claim 1, wherein the at least two dielectric layers in tension comprise a nitride layer and an oxynitride layer.

[c10] The process according to claim 1, wherein the dry etching step comprises simultaneously defining an infrared-absorbing body within the cavity and on the micromachined member.

[c11] The process according to claim 10, wherein the dry etching step comprises:
applying a mask to the surface of the substrate;
defining an opening in the mask;
dry etching the substrate through the opening in the mask using first etch conditions to define a trench surrounding a surface region of the substrate that remains unetched as a result of being protected by the mask;
removing the mask; and then
dry etching the trench and the surface region using etch conditions different than the first etch conditions until the trench stops at the oxide layer, a portion of the substrate remaining in the cavity to define the infrared-absorbing body surrounded by the trench.

[c12] The process according to claim 10, wherein the dry etching step comprises:
applying a mask to the surface of the substrate;
defining a first opening in the mask and a plurality of second openings in the mask that are smaller than the first opening, the first opening being continuous and surrounding the plurality of second openings; and then
dry etching the substrate through the first and second openings in the mask

using first etch conditions to define a trench that stops at the oxide layer and then using second etch conditions different than the first etch conditions to form the infrared-absorbing body surrounded by the trench.

[c13] A process of fabricating an infrared sensor comprising a circuit device and a diaphragm on a single semiconductor substrate that is not heavily doped, the process comprising the steps of:
forming the circuit device on the substrate by processing steps that include forming a thermal oxide layer on a surface of the substrate, forming a first tensioned dielectric layer on the thermal oxide layer, forming a thermal sensing layer over the first tensioned dielectric layer, forming at least a first conductive layer over the thermal sensing layer, and then forming a second tensioned dielectric layer so that the first conductive layer is between the first and second tensioned dielectric layers; and then
dry etching a surface of the substrate to form a cavity therein and thereby delineate the diaphragm and a frame surrounding the diaphragm, the dry etching step terminating at the thermal oxide layer, the diaphragm comprising the thermal oxide layer, the first and second tensioned dielectric layers, and the first conductive layer.

[c14] The process according to claim 13, wherein the diaphragm has a first surface for receiving thermal radiation and the sensing layer comprises at least one thermopile comprising a sequence of thermocouples, each thermocouple comprising dissimilar electrically-resistive materials that define hot junctions located on the diaphragm and cold junctions located on the frame, the first conductive layer defining metal conductors that electrically connect the thermopiles to the circuit device.

[c15] The process according to claim 13, wherein one of the dissimilar electrically-resistive materials is p-type doped polysilicon.

[c16] The process according to claim 13, wherein the cavity has a rectangular shape with rounded corners.

[c17] The process according to claim 13, wherein one of the first and second

tensioned dielectric layers is formed of a nitride and one of the first and second tensioned dielectric layers is formed of an oxynitride.

[c18] The process according to claim 13, wherein the first tensioned dielectric layer is formed of nitride and the second tensioned dielectric layer is formed of an oxynitride layer.

[c19] The process according to claim 13, wherein the dry etching step comprises:
applying a mask to a surface of the substrate opposite the circuit device;
defining an opening in the mask;
dry etching the substrate through the opening in the mask using first etch conditions to define a trench surrounding a surface region of the substrate that remains unetched as a result of being protected by the mask;
removing the mask; and then
dry etching the trench and the surface region using etch conditions different than the first etch conditions until the trench stops at the oxide layer, a portion of the substrate remaining in the cavity to define an infrared-absorbing body surrounded by the trench.

[c20] The process according to claim 13, wherein the dry etching step comprises:
applying a mask to a surface of the substrate opposite the circuit device;
defining a first opening in the mask and a plurality of second openings in the mask that are smaller than the first opening, the first opening being continuous and surrounding the plurality of second openings; and then
dry etching the substrate through the first and second openings in the mask using first etch conditions to define a trench that stops at the oxide layer and then using second etch conditions different than the first etch conditions to form the infrared-absorbing body surrounded by the trench.